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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
KAPADIA, VARSHA A	

ART UNIT	PAPER NUMBER
2627	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,433	POSS, JOE M.	
	Examiner	Art Unit	
	Varsha A. Kapadia	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Rejection Under 35 U.S.C. 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 10-11, 13-14, 19 and 25-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 10 and 13, line 2, the term "an can" is vague and lacks of antecedent basis. Furthermore, "a load" appears to have been recited in claim 1, therefore, it is unclear if this is a second load recited in claim 10 or is the same as claimed in claim 1.

In claim 19, last line "said circuit" lacks of antecedent basis. Line 2 recites a circuit and line 6 recites a circuit. Which one is the applicant trying to reference?

In claims 25 and 26, the term "said output node" lacks of antecedent basis.

In claims 10-11,13-14 and 26, the phrase "can be" as recited is vague and indefinite.

Rejection Under Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-27 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-29 of U.S. Patent No. 6,960,907 in view of Knight et al . (6,639,373).

The regulator circuit limitations recited in the claims 1-27 of the present application are similar to those recited in the claims 1-29 of the U.S.Patent 6,960,907. Claims 1-3, 12 and 19-20 of the present application further recite that the regulating circuit is connected to the hard disk device controller.

Knight et al. however, discloses hard disk device controller coupled to the regulating circuit (see fig. 2disclosure thereof and col.1 lines 11-22).

It would have been obvious to one of ordinary skill in the art at the time this invention made to modify the teachings of Poss et al (6,960,907) with the above teaching from Knight et al inorder to provide a capability to incorporate the regulating circuit in the hard disk device to enable de-latching of a head carriage by regulating sufficient magnitude of the voltage.

Rejection Under 35 U.S.C. 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pulkin et al (US 6,573,694) in view of Knight et al (6,639,373).

With regards to claims 1-3 and 7-15, Pulkin et al disclose an electronic device (see col.1 lines 9-10) comprising a linear regulator circuit comprising: a circuit control node (22); a circuit output node (Vout) to which a load is connected (load), a voltage at the circuit output node being determined based on a voltage signal at the circuit control node; an amplifier circuit (24) having a first amplifier input and a second amplifier input, and further having an amplifier output, the first amplifier input configured for receiving a reference voltage (VREF), the amplifier circuit (24) receiving power from a first voltage source (Vs); a source follower circuit (34) having a source follower input node and a source follower output, the amplifier output configured drive the source follower input node, the source follower output coupled to the circuit control node; and a feedback circuit (26,28) coupled between the circuit output node and the second amplifier input. Pass element (22). Current source (32).

Pulkin et al fails to further disclose that the regulator circuit is coupled to the hard disk device controller.

Knight et al. however, disclose hard disk device controller coupled to the regulating circuit (see fig. 2disclosure thereof and col.1 lines 11-22).

It would have been obvious to one of ordinary skill in the art at the time this invention made to modify the teachings of Pulkin et al with the above teaching from Knight et al inorder to provide a capability to incorporate the regulating circuit in the hard disk device to enable de-latching of a head carriage by regulating sufficient magnitude of the voltage.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pulkin et al (6,573,694) in view of Knight et al (6,639,373). as applied to claims 1-3 and 7-15 above, and further in view of Hsiao et al (3,984,780).

Pulkin et al and Knight et al disclose the claimed subject matter in regards to claims 1 and 12 supra, except for a current mirror coupled between the amplifier and the source follower.

Hsiao et al teaches a source follower (4) and an amplifier (2) having a current mirror coupled (32) therebetween for mirroring the current from the amplifier to regulate the output voltage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Pulkin et al in view of Knight et al to include a current mirror coupled between the amplifier and the source follower for mirroring the amplifier current and regulating the output voltage as taught by Hsiao et al.

Claims 5-6 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pulkin et al (6,573,694) in view of Knight et al (6,639,373) and Hsiao et al (3,984,780) as applied to claims 1-4 and 7-15 above, and further in view of Miranda et al (5,631,598).

Pulkin et al in view of Knight et al and Hsiao et al disclose the claimed subject matter in regards to claims 1 and 12 supra, except for a resistor component coupled between a voltage source and the source follower input.

Miranda et al teach connecting a resistor component (R3,R4) between a voltage rail and a transistor for among other things restricting current to the transistor and dividing the source voltage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Pulkin et al in view of Knight et al and Hsiao et al to include a resistor component coupled between a voltage source and the source follower input in order to restrict current therethrough or to divide the source voltage to a proper voltage for the source follower input.

Claims 19-20 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pulkin et al (US 6,573,694) in view of Knight et al (6,639,373) and Xi (6,246,221).

With regards to claims 19-20 and 25-26, Pulkin et al disclose a device (see col.1 lines 9-10) comprising a linear regulator circuit comprising: an amplifier circuit (24) having a first amplifier input and a second amplifier input, and further having an amplifier output, the first amplifier input configured for receiving a reference voltage (VREF), the amplifier circuit (24) receiving power from a first voltage source (Vs); a source follower circuit (34) having a source follower input node and a source follower output, the amplifier output configured drive the source follower input node, the source follower output coupled to the circuit control node; and a feedback circuit (26,28) coupled between the circuit output node and the second amplifier input. Pass element (22).

Pulkin et al fails to further disclose that the regulator circuit is coupled to the hard disk device controller.

Knight et al. however, discloses hard disk device controller coupled to the regulating circuit (see fig. 2disclosure thereof and col.1 lines 11-22).

It would have been obvious to one of ordinary skill in the art at the time this invention made to modify the teachings of Pulkin et al with the above teaching from Knight et al inorder to provide

a capability to incorporate the regulating circuit in the hard disk device to enable de-latching of a head carriage by regulating sufficient magnitude of the voltage.

Pulkin et al in view of Knight et al do not disclose a bandwidth at the output node has a pole at a frequency greater than the unity gain frequency of the circuit.

Xi teaches an output amplifier stage having a pole associated therewith, the output amplifier stage configured to receive the amplified displacement circuit signal such that the pole associated with the output amplifier stage is pushed out to a frequency above the Unity Gain Frequency of the compensation loop thereby rendering the voltage regulator output stage capable of generating a stable regulated output voltage at frequencies in the vicinity of the control loop bandwidth associated with the voltage regulator.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Pulkin et al in view of Knight et al to include a bandwidth at the output node has a pole at a frequency greater than the unity gain frequency of the circuit as taught by Xi in order to render the voltage regulator output stage capable of generating a stable regulated output voltage at frequencies in the vicinity of the control loop bandwidth associated with the voltage regulator.

Claims 21-24 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pulkin et al (6,573,694) in view of Knight et al (6,639,373) and Xi et al (6,246,221) as applied to claims 19-20 and 25-26 above, and further in view of Miranda et al (5,631,598).

Pulkin et al in view of Knight et al and disclose the claimed subject matter in regards to claims 19-20 and 25-26 supra, except for a resistor component coupled between a voltage source and the source follower input.

Miranda et al teach connecting a resistor component (R3,R4) between a voltage rail and a transistor for among other things restricting current to the transistor and dividing the source voltage.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Pulkin et al in view of Knight et al and Xi et al to include a resistor component coupled between a voltage source and the source follower input in order to restrict current therethrough or to divide the source voltage to a proper voltage for the source follower input.

Conclusion

Reference to Somerville et al (6,586,987) cited as of interest.

Reference to Perez (6,646,495) cited as of interest.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Varsha A. Kapadia whose telephone number is (571) 272-7557. The examiner can normally be reached on Mon Tue and Thurs. from 6:30 AM to 2:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrea Wellington can be reached on 571 272 4483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VK

ANDREA WELLINGTON
SUPERVISORY PATENT EXAMINER